GOVERNMENT COLLEGE (AUTONOMOUS), RAJAHMUNDRY

(Accredited by NAAC "A+" Grade)

DEPARTMENT OF COMPUTER SCIENCE & APPLICATIONS

I B.Sc. Semester-II

Digital Logic Design

MODEL QUESTION PAPER (W.E.F 2023-2024)

Time: 2 ½ Hrs. **Max Marks: 50 M**

SECTION - I

Answer any FIVE questions **5 X 3= 15M**

1. Explain about r's Complement and (r-1)'s complement.
2. Convert $(45)_{10}$ to binary and hexa decimal number.
3. Write a short note on Universal gates.
4. Write a truth table for X-NOR and X-OR gates.
5. Write a short note on half subtractor.
6. Write a short note on half adder.
7. Write a short note on decoders with example.
8. Write a short note on multiplexer with example.

SECTION - II

Answer the following questions **5 X 7 = 35M**

9. Explain in detail about weighted and weighted codes.

(OR)

10. Binary, octal, decimal, hexadecimal number systems.

11. Explain about Product of Sums and Sum of Products with example.

(OR)

12. Explain Boolean laws and theorems.

13. Explain about ripple adder/subtractor with example

(OR)

14. Explain about Full adder and full subtractor with example.

15. Design 3 X 8 decoder with two 2 X 4 decoders.

(OR)

16. Design 4 X 1 and 8 X 1 multiplexer with examples.

17. Explain about RS Flip Flop and JK Flip Flop with example.

(OR)

18. Explain about Bidirectional shift register and universal shift register with example.